ABSTRACT

In a SONET/SDH network the frame alignment is an important function. This paper presents a component that realizes it and the section layer functionality in a SONET/SDH network. The user can choose between STS-1/STM-0 at 51.48 Mbps or STS-3/STM-1 at 154.44 Mbps operation. There are some components to do frame alignment [1] but here we present a new component with a wider range of functions. The proposed circuit consists of a parallel descrambler, a section alarms indicator and section BIP-8 byte calculator. We introduce all these functions in only one component. This framer can be part of any network element (NE) with section layer function. Moreover, it works with byte flow instead of bit flow. This component can be reused for construction of a framer at higher transmission rate.

1. INTRODUCTION

We present a configurable framer and overhead bytes processor in section layer for SONET/SDH. SONET/SDH are a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks [4,7].

The component presented here will be part of a library for SONET/SDH [1,2, 7, 9, 10] in development at the Center of Research and Advanced Studies of IPN, at Guadalajara, Mexico. That allows to implement network elements in a short time, just like the 2.5 Gbps SONET STS-48/SDH STM-16 Add/Drop Multiplexer [3] in development in our Center.

Likewise, we present a proposed architecture to achieve higher transmission rates, like STS-48/STM-16 or higher. Finally, we present the conclusions about functional verification of the design for STS-3/STM-1 signals.

Main objectives of this work are the requirement specification, architecture and verification of the design. We will show how the framer is divided into blocks and we explain the functionality and structure of every block.

2. GENERAL CHARACTERISTICS

This configurable framer with section layer functionality for SONET/SDH operates with STS-1/STM-0 or STS-3/STM-1 byte data stream (according to the configuration).

Figure 1. SONET/SDH STS-3/STM-1 framer

This component is named commonly framer. It receives SONET/SDH scrambled data stream and deliver byte SONET/SDH data stream, according to the configuration, with or without scrambling, see Figure 1.

The framer is divided into four related sub-modules (figure 2):

?? Frame aligner with byte delimiter.
?? Section alarms indicator block.
?? Descrambler.
?? Section BIP-8 calculator block.

Figure 2. Framer blocks diagram

This byte processor in the reception side (Rx) operates with STS-1/STM-0 or STS-3/STM-1 (according to the configuration).
3. FUNCTIONALITY

3.1 Frame Aligner with Byte Delimiter Functionality

1. To declare frame aligned.
2. To declare Out of Frame (OOF).
3. To align bytes for STS-1/STM-0 STS-3/STM-1 byte data input stream.
4. To generate frame pulse (FP).
5. To indicate byte J0.
6. To indicate last byte of frame.

3.2 Section Alarms Indicator Device Functionality

7. To produce Loss Of Frame (LOF) [5].
8. To produce Loss Of Signal (LOS) [5].
9. To produce Loss Of Clock (LOC) [5].

3.3. Descrambler Functionality

10. To deliver byte data output stream with or without descrambling.

3.4 Section BIP-8 Calculator Device Functionality

11. To calculate section BIP-8 byte.

4. SUBMODULES DESCRIPTION

4.1 Frame Aligner

The frame aligner is a SONET/SDH block. It searches the FSC (frame synchronous code) A1A2 for STS-1/STM-0 or A1A1A2A2A2 for STS-3/STM-1 with the purpose of frame alignment. Here A1=”11110110” (Hex F6) and A2=”00101000” (Hex 28) [8].

The FSC must appear every 125 μs, because it is the duration of a complete frame. When the beginning of a frame is detected, the frame aligner generates a pulse named frame pulse (FP). Knowing FP location is easy to define the J0 byte location, because J0 byte is next to the last A2 byte of FSC. Frame aligner produces other pulse, different to FP, when J0 byte is detected.

A SONET NE shall be aligned with others NE’s. When the frame aligner detects two consecutive FP (or four, according to the configuration), aligned frame is declared. Framing monitoring is done in the communication process to find the possible loss of aligned frame. The state loss of alignment is named Out Of Frame (OOF). An OOF signal is detected when the incoming SONET/SDH signal has four consecutive errored framing patterns.

Framer identifies also the end of each transmitted frame. This is an additional function implemented to begin the section BIP-8 calculation.

4.2 Byte Delimiter

The frame aligner contains a byte delimiter. This circuit limits the byte bounds in SONET/SDH data input. Data input is a serial flow of bytes (8 bits each clock pulse), which is obtained randomly. Consequently, the probability to find a delimited byte correctly is very small. For instance, if the circuit is receiving, in a STS-1 frame, A1 and A2. The most probable case is to receive a part of A1, then the rest of A1, and so on with A2 and J0. Figure 3(A) shows the ideal case when the bytes data input are delimited in bounds. Figure 3(B) shows a more realistic case.

4.3 Section Alarms Indicator Device

This block detects the following defects in the section layer: loss of signal (LOS), loss of frame (LOF) and loss of clock (LOC). Figure 4 shows the inner block diagram of this device.

4.3.1 Loss of frame (LOF)

The incoming SONET/SDH signal is monitored for LOF defect. A SONET/SDH detects an LOF defect when an OOF defect on the incoming SONET/SDH signal persists for 3ms (24 consecutive frames).
The framer ends an LOF defect when the NE recovers synchronization. In SONET/SDH an LOF detection begins for maintenance such as AIS and RDI.

4.3.2 Loss of signal (LOS)
To detect an optical or physical failure, just like laser failure or fiber cut, the incoming SONET/SDH signal is monitored for loss of signal. The detection of an LOS defect must occur within a reasonably short period of time for timely restoration of the transported payloads.

A SONET/SDH NE monitors all incoming signal (before descrambling) for an “all-zeros byte patterns”. An “all-zeros byte” is “00000000”. An all-zeros pattern corresponds to no light pulses for OC-N optical interfaces and no voltage transitions for STS-N/STM-M electrical interfaces. An LOS defect shall be detected when an all-zeros pattern lasts 1000 s.

4.3.3 Loss of clock (LOC)
An LOC defect is not defined in SONET/SDH standards; however, in the framer presented here this function is implemented. Detection of an LOC defect principally consists in monitoring the main system clock to verify loss of clock transitions. An LOC defect is detected when the system misses 4 clock cycles consecutively. To do this it is necessary the employment of a second clock and to divide the frequency of the principal signal clock. With the second clock the LOC detector (Figure 4) searches loss of pulses (see Figure 5).

Division of clock is done to make easy the detection of missed pulses.

The framer ends an LOC defect when it detects a new clock pulse of the principal clock.

4.4 Descrambler
SONET/SDH optical interface signal use binary line coding, and therefore must be scrambled to assure a certain number of transitions (zeros to ones, and ones to zeros) for purposes such as line rate clock recovery at the receiver. SONET/SDH electrical interfaces signal use line codes that assure adequate transitions (i.e., B3ZS and CMI). However, they are also scrambled for consistency between the electrical and optical interfaces. In both cases, the used scrambler is a circuit that can be applied identically at the transmitter and the receiver. The descrambler operation is an inverse operation of the scrambler [8].

The framer showed in this paper contains an internal descrambler. In Figure 6 is presented the parallel architecture used to implement the descrambler. This architecture is similar to the parallel descrambler presented in other documents [11].

The descrambler is divided into three components: a shift register array (parallel input/parallel output), a feedback circuit and a descrambler output array.

![Figure 6. Descrambler Architecture](image)

The descrambler here presented has the following characteristics:

1. A frame-synchronous descrambler of sequence length 127 operating at the line rate [8].
2. Since the generating polynomial is given by $P(x)=1+x^6+x^7$, there are seven one-bit memory devices, such as shift register, used in this SONET/SDH descrambler [8].
3. This scrambler is reset by the first bit of the byte following the last byte of the first row section overhead [8].
4. The descrambler must run continuously throughout the complete STS-N/STM-M frame [8].
5. The frame bytes A1 and A2 and J0 byte are not descrambled [8].

Equations of the feedback circuit are given by:

- \( D_0 = Q_1 + Q_2 \)
- \( D_1 = Q_2 + Q_3 \)
- \( D_2 = Q_3 + Q_4 \)
- \( D_3 = Q_4 + Q_5 \)
- \( D_4 = Q_5 + Q_6 \)
- \( D_5 = Q_6 + Q_7 \)
- \( D_6 = Q_0 + Q_2 \)

And the logic combinations in the descrambler output arrays are:
This output sequence is added module 2 to the SONET/SDH data stream (Figure 6).

4.5 Section BIP-8 Calculator Device

This framer sub-module has the principal task of calculating the section BIP-8 byte of the incoming SONET/SDH signal. It calculates the parity of SONET/SDH frame.

There are 8 counters for B1 calculation. The first one is used to calculate the parity of all first bits position from all bytes of SONET/SDH frame. Another will repeat the same procedure for the 2nd, 3rd, ..., and the 8th bit position of all bytes of SONET/SDH frame [8].

The generated last byte of frame indicates to the circuit the beginning of B1 calculation.

This framer does not compare the B1 here calculated with the one obtained in the previous frame. This is function of the RSOH processor [2].

5. FRAMER STS-48/STM-16 BASED IN FRAMER STS-3/STM-1

Now, we present a proposed architecture for a framer STS-48/STM-16 based on STS-3/STM-1 framer which was presented in this paper. Figure 8 shows this architecture.

With some modifications in the framer and with a new architecture based on STS-3/STM-1 framers, we can to build a framer SONET/SDH STS-48/STM-16. The proposed architecture needs 16 aligners with byte delimiter STS-3/STM-1. In this case, the FSC have 48 A1 bytes and 48 A2 bytes. We propose a 16 bits bus to connect the sub-modules of framer. Each aligner must detect three A1 bytes and three A2 bytes. If it is necessary, SONET/SDH aligned data stream must be delivered to a 16-bit bus (see Figure 8).

The rest of the modules must be modified to 16-bit bus. The descrambler must be expanded to deliver 16 descrambled bits instead of 8 bits. For that, it is necessary to modify the equations presented above. The section alarms indicator device and the section BIP-8 calculator must be instanced 16 times.

6. VERIFICATION

For the verification process some testbenches were implemented using VHDL. The circuit was timing verified. For the individual verification of frame aligner, we found a satisfactory operation for STS-3/STM-1; but it needs some modification to achieve higher transmission rates (for futures versions).

Individually, the parallel descrambler and the section BIP-8 calculator work till STS-12/STM-4 signals and with an easy modification can achieve higher rates (for futures versions).

The blocks of all codes were simulated to verify the fulfillment of all framer requirements obtaining satisfactory results. The code of this component will be part of a library SONET/SDH to future works in our institution.

7. CONCLUSIONS

A SONET/SDH framer for STS-3/STM-1 signals was built. This framer presents a parallel architecture to improve performance, working with a bus of 8 bits, instead of a serial bit stream.

Also, this framer can be used as base module to build others at higher speed rates, just like STS-48/STM-16.
Although, all blocks, of the framer, will suffer modifications to achieve this objective.

8. REFERENCES


