IMPLEMENTATION OF A PROGRAMMABLE HIGH SPEED DIVIDER FOR A 2.4 GHZ CMOS INTEGER-N FREQUENCY SYNTHESIZER

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SUMMARY

The design of a programmable high speed divider for a RF Frequency Synthesizer using CMOS 0.35 µm technology (four metal levels and 2 poly levels) is presented. The Frequency Synthesizer employs the integer-N architecture, and it aims at the ISM band (Industrial, Scientific and Medicine) with the nominal frequency of 2.4 GHz. The divider is composed of: a dual-modulus prescaler, a main counter, a swallow counter, and the control logic required to provide the correct operation. The most demanding block in terms of speed in the divider is the dual-modulus prescaler, because it has to work with the maximum operating frequency. For its implementation the E-TSPC (Extended True Single Phase Clock) technique was used showing good results with high operating speed. In addition to the divider, a complete Synthesizer was also designed to test the divider; it includes a VCO, a phase frequency detector with charge pump, a low pass filter, buffers to increase the signal levels, and the programmable divider itself.

In this paper, the different parts forming the divider are explained in detail, from the basic cells that originate the prescaler to the state diagrams of the prescaler synchronous counter. Also, it is explained how to program the Synthesizer to obtain sixteen different output frequencies. Some simulations results, based on the layout extracted netlists, are presented. The simulations are done with ELDO 5.6, Mentor Graphics, transistor model BSIM3v3, and typical parameters. The programmable high speed divider reaches a maximum frequency of 2.75 GHz and power consumption of 5.6 mW with 3.3V power supply and 198 µm x 33 µm area.

RESUMEN

El diseño de un divisor programable de alta velocidad para un Sintetizador de Frecuencia para RF utilizando tecnología CMOS de 0.35 µm (cuatro niveles de metal y 2 niveles de poli) es presentado. El Sintetizador de Frecuencia emplea la arquitectura integer-N, y está proyectado dentro del estándar ISM (Industrial, Scientific and Medicine) con frecuencia nominal de 2.4 GHz. El divisor se compone de: un prescaler dual-modulus, un contador principal, un contador swallow, y la lógica de control necesaria para la correcta operación. El bloque más demandante en términos de velocidad en el divisor es el prescaler dual-modulus, ya que tiene que trabajar con la frecuencia de operación máxima. Para su implementación la técnica E-TSPC (Extended True Single Phase Clock) fue usada mostrando buenos resultados, para velocidades de operación altas. Además del divisor, un Sintetizador completo fue diseñado para probar el divisor; él incluye un VCO, un detector de fase y frecuencia con bomba de carga, un filtro pasa bajos, buffers para amplificar los niveles de las señales, y el propio divisor programable.

En este paper, las diferentes partes que forman el divisor son explicadas en detalle, desde las celdas básicas que originan el prescaler hasta los diagramas de estado del contador sincrónico del prescaler. También, se explica como programar el Sintetizador para obtener 16 diferentes frecuencias. Algunos resultados de simulación, basados en los netlists extraídos del layout, son presentados. Las simulaciones fueron realizadas con ELDO 5.6, de Mentor Graphics, con modelo de transistor BSIM3v3, y con parámetros típicos. El divisor programable de alta velocidad alcanza una frecuencia máxima de 2.75 GHz, un consumo de potencia de 5.6 mW con una fuente de alimentación de 3.3 V y ocupa un área de 198 µm x 33 µm.
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ABSTRACT

The implementation of a programmable high speed divider for a CMOS Frequency Synthesizer, using 0.35 µm CMOS technology, is described. The Frequency Synthesizer is part of a RF transceiver to work in the 2.4 GHz ISM (Industrial, Scientific and Medicine) band. The programmable divider employs: a divide-by-32/33 dual-modulus prescaler composed by a divide-by-4/5 synchronous counter, using the Extended True Single Phase Clock (E-TSPC) technique, and a divide-by-8 asynchronous counter; two other counters, a fixed and a descending programmable (swallow) counter; and the necessary control logic to operate the divider.

Additionally, a complete Synthesizer was fully designed to test the divider; it includes a VCO, a phase frequency detector with charge pump, a low pass filter, buffers to increase the signal levels, and the programmable divider itself. The results obtained by means of layout simulations show a maximum frequency of 2.75 GHz and power consumption of 5.6 mW with 3.3V power supply. The programmable divider has 198 µm x 33 µm and the prescaler has 77 µm x 33 µm.

1. INTRODUCTION

Frequency synthesizers have been used for many years in analog and digital electronic applications. In communication systems they are employed in transceivers to select the operation frequency of the transmitter and the receiver (see Fig. 1), to tune to different frequency channels of the communication band [1], [2].

Due to the high accuracy required in the value of the output frequency of the frequency synthesizers, the dominant architecture for them is based on phase-locked loops (PLLs) [2]. Additionally, the frequency output can be adjusted in very precise steps (Fig. 2) with the use of a programmable divider in the feedback loop of the PLL. Between the different divider architectures, those that use a dual-modulus prescaler are very popular due to their versatility and facility of implementation [3].

In former years the most used technologies for high speed dividers were bipolar and GaAs. Nowadays, CMOS technology has also been employed with the advantages of cost, integration level and power consumption.

The design of a programmable high speed divider using a 0.35 µm CMOS process (see Table 1 for the process details) is presented in this work. The divider has a dual modulus prescaler 32/33, two counters, the main counter and the swallow counter, and the necessary control logic that allows the selection of the desired division factor. Furthermore, in order to test the divider, a complete Integer-N Architecture 2.4 GHz Frequency Synthesizer is also designed. It includes a LC tank oscillator (VCO), a phase frequency detector with charge pump, a low pass filter, buffers to increase the signal levels, and the programmable divider with the prescaler. From these blocks, the VCO and the prescaler are the blocks that require more attention since they operate with the maximum speed, 2.4 GHz.

One of the main aims of this work is to offer detailed information about how to design the programmable divider, what is hardly found in the literature: details about the prescaler, about the logic control of the counters, and even about how to choose the divide factors.

Table 1. AMS 0.35 µm CMOS Process Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply VDD</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Minimum Gate Length L</td>
<td>0.35 µm</td>
</tr>
<tr>
<td>Gate Oxide Thickness T_ox</td>
<td>7.6 nm</td>
</tr>
</tbody>
</table>

This work was supported in part by CNPq and FAPESP, Brazil.
The remainder of this paper is organized as follows: in section 2 some theoretical aspects about the programmable divider architecture will be developed; in section 3 the projected building blocks will be described; in section 4 the application of the divider in a frequency synthesizer will be shown; finally, in section 5 some comparisons with other jobs and conclusions are presented.

2. THEORETICAL CONSIDERATIONS

A frequency synthesizer can be seen as a PLL that incorporates a divider in its feedback path (see Fig. 2). The operation of the divider in the frequency Synthesizer is as follows: initially the two counters, the main counter and the swallow counter, are set with the values P and S, respectively, where S ≤ P and the S value is externally controlled. The signal modulus control is set to high and, in this case, the prescaler, that receives the clock fosc from the VCO, will divide it by V+1. The two counters count down with the prescaler output until the swallow counter reaches zero. At this moment the modulus control signal is set to low, the prescaler starts dividing by V, and the main counter starts counting with \((f_{osc}/V)\) clock up to reach zero. At this point the two counters will be reset and the full process begins again. Thus, during the full process, the prescaler divides the VCO clock S times by \((V+1)\), and \((P-S)\) times by \(V\). The total division factor of the divider will be: \(N=(V+1)S + V(P-S) = VP + S\). When the synthesizer is locked, the output frequency of the VCO is: \(f_{osc}=Nf_{ref} = (VP+S)f_{ref}\).

As a result, the output frequency of the VCO can be controlled by means of the programmed value \(S\) in the swallow counter.

The VCO used in our implementation is a fully differential with a single control input, designed using on-chip spiral inductors, varactors, and a cross-coupled differential pair \((M_1, M_2)\) as a negative resistance for the LC resonator as shown in Fig. 3.

3. BUILDING BLOCKS

3.1. Prescaler

From the early days of the CMOS technology up to the present, several CMOS clock policies have been proposed. Between them, single-phase-clock policies are superior with respect to the clock distribution and present lower wirings costs and requirements (no problems with phase overlapping, etc.). Consequently, higher frequencies and simpler designs can be achieved with them.

Introduced by [4] and [5], the extended true-single-phase clock CMOS circuit technique (E-TSPC), an extension of the TSPC, consists of composition rules for single-phase circuits using static, dynamic, latch, data-precharged, and NMOS-like blocks. The composition rules are introduced to enlarge the block-connection possibilities and avoid races; additionally, NMOS-like blocks enhance the technique for high-speed operations.

The dual-modulus prescaler (divide by 32/33) of this work is implemented with the E-TSPC technique [6]. Figure 4 shows the prescaler schematic. Two parts can be identified in the diagram: the first part, inside the cross-hatched box, is composed of three fall edge-triggered D-flip flops (D-FF) and two logic gates, and forms a synchronous divide-by-4/5 counter [see the timing diagram in Fig. 5 (a)]; the other, at the bottom of the figure, is composed of three rise edge-triggered D-FFs and forms an asynchronous divide-by-8 counter. The div8 signal, generated by the asynchronous counter, selects if the divide-by-4/5 counter counts up to 4 (\(\text{div8} = \text{high}\)) or up to 5 (\(\text{div8} = \text{low}\)). The fractional division...
The ratio of the prescaler, 32 or 33, is selected according to the \( sm \) signal value.

In Fig. 5 (a) and Fig. 5 (b) the timing and transition diagrams respectively are depicted. The transition diagram presents the different states that the synchronous divide-by-4/5 counter will have for each clock signal (output of the VCO), according to the value of \( div8 \). The state values are represented by the D-FFs output values, signals A, B and C shown in Fig. 4. When the circuit goes through the states 111, 101, 000 or 001, and 011 the division by 4 operation is performed; when it goes through 111, 101, 000 or 001, 010, and 011 the division by 5 is performed (notice that the signal \( A \) provides the divided signal). The decision about counting up to 4 or 5 is done at states 001 or 000 and the decision depends on the value of signal \( div8 \). Fig. 5 (a) indicates the values of \( div8 \) and the instant that they should be provided to guarantee the correct operation: for counting 4 the signal \( div8 \) should has “high” value at states 000 or 001; for counting 5, “low” value at state 000 or 001. Since the counting decisions are done at states 001 or 000, usually they are the most critical in terms of timing.

The signal A will be used as the clock input of the asynchronous divide-by-8 counter. The outputs of the D-FFs of this counter (signals \( ckn8 \), \( ckn16 \) and \( ckn32 \)) and the signal \( sm \) are the inputs of the logic port NAND whose output is the signal \( div8 \). When \( sm \) is “low” the output of the NAND will always be “high” and the divide-by-4/5 counter will keep dividing by 4. When \( sm \) is “high” the output of the NAND will depend on the signals \( ckn8 \), \( ckn16 \) and \( ckn32 \). If these signals are simultaneously “high” then the signal \( div8 \) will be “low” and the divide-by-4/5 counter will divide by 5.

Observe that the selections of rise edge-triggered D-FFs and of the signal A as the clock (B signal could be also used) in the asynchronous counter are the best to produce the \( div8 \) signal with the desired timing requirements. With such configuration, modifications in \( div8 \) are initialized during the transitions from state 011 to 111, and, since the \( div8 \) is only important at the end of 000 or 001 states, a delay of almost three clock periods is allowed for the signal.

An adapted version of the conventional fall edge-triggered TSPC D-FF [7] was used at the synchronous counter. This cell has the advantage of reaching higher frequencies at the expense of power consumption. The Fig. 6 (a) depicts the D-FF connected as a divide-by-2 counter, and Fig. 6 (b), its signals during a divide-by-two operation. The dimensions of the P and N transistors have to obey several requirements to guarantee the correct operation. They are: when both transistors M1 and M2 are simultaneously on, the output \( a \) must be “high”; when both transistors M3 and M4 are simultaneously on, the output \( b \) must be “low”; and when both transistor M5 and M6 are simultaneously on, the output must be “low”.

The optimal dimensions of the transistors were calculated and adjusted by simulations. An additional requirement was considered in this case: to keep the dimensions as small as possible to maintain the power consumption low. Fig. 7 shows the simulation results for the D-FF connected as a di-
vide-by-2 counter. The simulation was performed with ELDO 5.6, transistor model BSIM3v3, typical parameters, and the netlist extracted from the layout [compare the signals with Fig. 6 (b)]. For this circuit, the maximum operation frequency is 2.75 GHz for power supply of 3.3V.

After obtaining this basic cell, the rest of the prescaler was designed and it is depicted in Fig. 8 with all transistor sizes. The dimensions of the synchronous counter transistors were determined based on the adapted D-FF. For the asynchronous counter, after several simulations, it was found that the conventional TSPC D-FF is fast enough, and we determined its optimal dimensions. Finally a NAND employing transistors with minimal dimensions is applied to generate the \( \text{div8} \) signal. Notice that the signal \( \text{sm} \) is only connected to one P Transistor of the NAND; the goal of this is to avoid using 4 N transistors in series at the output what would reduce the port speed.

The layout of the complete prescaler is presented in Fig. 9. The synchronous counter can be seen on the left of the figure, and the asynchronous counter, on the right. It is also possible to see a guard ring around the synchronous counter whose function is to reduce the switching noise introduced into the substrate. This noise is particularly harmful to the oscillator, in the frequency synthesizer, and to other analog blocks in a system.

In Fig. 10, the simulation of the divide by 4/5 counter is presented. We can see that when the \( \text{div8} \) signal is “high” the counter divides by 4, and when it is “low”, divides by 5.

In Fig. 11, the simulation of the asynchronous part of the prescaler is depicted for the case when \( \text{sm} = \text{“high”} \).

3.2. Main Counter
It was seen that one of the counters, the main counter, works with a fixed counter limit value, and the other, the swallow counter, with a programmable limit value. Due to such configuration, the divider programmed factor and, consequently, the synthesizer frequency are adjusted by setting

Fig. 7. Simulation results of the basic D-FF for the prescaler. ELDO 5.6, transistor model BSIM3v3, typical parameters were used and the D-FF reached a 2.75 GHz maximum frequency.

Fig. 8. Transistor schematic of the prescaler. The transistor width or, when the length is different from 0.35 \( \mu \)m, the transistor width/length in \( \mu \)m, is also indicated in the figure.

Fig. 9. Layout of the prescaler (tecnologia AMS CMOS 0.35 \( \mu \)m C35B4/CSI)

Fig. 10. Simulation of the divide-by-4/5. ELDO 5.6, transistor model BSIM3v3, typical parameters.
the swallow counter limit.

The main counter was implemented with four conventional TSPC D-FFs in cascade, similarly to the asynchronous part of the prescaler, and it counts up to 16 (Fig. 12).

3.3. Swallow Counter

The swallow counter is basically a descendent programmable counter and its operation is as follows: first the counter is initialized with a value between 0 and 15, and, after that, it starts to count in descending way up to zero. When the value zero is reached, the counter is initialized again and the counter will be ready to start once more the operation. By means of the initial value it is possible to obtain 16 different frequencies separated by \( f_{ref} \) MHz.

There are different configurations in the literature to implement this counter. The architecture presented in Fig. 13 [8] was applied. In this counter, the signals \( I_A, I_B, I_C \), and \( I_D \) set the initial value that the counter uses to start the counting; the signal /lo controls if the values \( I_A, I_B, I_C \), and \( I_D \) are charged, /lo = "low", or if the counter is counting, /lo = "high".

Again, it was used the conventional TSPC D-FF.

3.4. Control Logic

We explained how the programmable divider should work in the synthesizer frequency, and now we will explain how the control logic circuit drives the different signals so the divider functions as expected. The control implemented in this work consists basically of a multiplexer and a four inputs OR (see fig. 14).

The control logic operation is as follows: starting the analysis by the output of the swallow counter, if in the first clock cycle all of its outputs are zero, then the OR output will also be zero. As a result, /lo = "low", the swallow counter is initialized with the \( (I_A...I_D) \) values, and immediately the OR output is forced to "high". The initialization process is interrupted. With \( sm=/lo= "high" \), the prescaler will divide by 33. The swallow counter will receive as clock the pulses coming from the output of the prescaler (by means of the multiplexer \( \text{mux} \)). When the swallow counter reaches zero, \( sm=/lo= "0" \), the prescaler will divide by 32, and the clock of the swallow counter will be the output of the main counter that is still zero. In this moment, the swallow counter has the signal /lo = "0", waits the output pulse of the main counter to initialize with the data \( (I_A...I_D) \), and starts the counting again.

In Fig. 15, the layout of the complete programmable divider is presented. The asynchronous counter of the prescaler, the main counter, the swallow counter and the logic control are placed as close as possible to avoid delays in the
signal paths. The synchronous counter is isolated on the left.

The simulation of the Control Logic is depicted in the Fig. 16. The datas programmed in the swallow counter using the inputs \( I_A = \text{"high"}, I_B = \text{"high"}, I_C = \text{"high"}, \) and \( I_D = \text{"low"}. \) With these datas \( S=7 \) and \( N=519. \)

It could be seen that initially the two counters (main counter and swallow counter) are set at the same time (swallow counter with \( S=7 \) and main counter with \( P=16 \)); while the swallow counter is counting, the multiplexer output is equal to the prescaler output; otherwise, when the swallow counter stops, the multiplexer output is equal to main counter output.

**4. APPLICATION: FREQUENCY SYNTHESIZER**

The programmable divider was applied in a frequency synthesizer that generates 16 output signals, sweeping from 2.4 GHz to 2.47 GHz. The complete layout of the circuit is presented in Fig. 17. We can see the divider inside the whole synthesizer.

According to Fig. 2, the synthesizer works as follows: the output frequency of the VCO should be kept with a constant desired value. This frequency is divided and its value is compared to the reference frequency \( (f_{ref}) \) by the phase frequency detector (PFD). The measured error is filtered by a low pass filter (LPF) that delivers a constant voltage to the VCO control. This process is continuous and, with the proper PFD and LPF design, the desired output frequency is achieved.

The power consumption of the frequency synthesizer should be low since it will be employed with portable RF systems. The complete programmable divide circuit consumes as much as 5.6 mW, distributed among

- the synchronous counter of the prescaler, 1.03 mW;
- the asynchronous counter of the prescaler, 1.00 mW;
- the main counter, swallow counter, and control logic, 3.57 mW.

**5. CONCLUSIONS**

It was presented the study of a programmable divider to be used in frequency synthesizers and implemented in a 0.35 µm CMOS process. The synthesizer is part of 2.4 GHz transceivers.

The divider has a prescaler resulted from a prior study of the E-TSPC technique [6], which is an extension of a TSPC technique. Additionally, the divider has a main counter, a swallow counter and control logic. The complete divider circuit attained 2.75 GHz and power consumption of 5.6 mW with 3.3 V.

The frequency synthesizer was designed using this divider and were simulated for different values of the division factor of the swallow counter, demonstrating the correctness of the control logic applied and the practical utility of the E-TSPC techniques developed in prior works [4], [5].

In Table 2 is presented one comparison of the present results for the prescaler and other results found in the literature (the prescaler is considered the most critical block of the divider, and there are not enough information about other complete dividers in the literature to draw comparisons). We can see that the results found in this work are good for both, speed and power consumption.
Table 2. Comparison of different prescaler works.

<table>
<thead>
<tr>
<th>Work</th>
<th>Technology (μm)</th>
<th>Power Supply (V)</th>
<th>Maximum Frequency (GHz)</th>
<th>Power Consumption (mW/GHZ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>0.25</td>
<td>2.5</td>
<td>2.5</td>
<td>14*</td>
</tr>
<tr>
<td>[10]</td>
<td>0.36</td>
<td>3.3</td>
<td>1.9</td>
<td>1.52</td>
</tr>
<tr>
<td>[11]</td>
<td>0.7</td>
<td>3</td>
<td>1.3</td>
<td>7.46</td>
</tr>
<tr>
<td>[12]</td>
<td>0.35</td>
<td>3</td>
<td>2.5</td>
<td>2</td>
</tr>
<tr>
<td>This work</td>
<td>0.35</td>
<td>3.3</td>
<td>2.75</td>
<td>0.74**</td>
</tr>
</tbody>
</table>

*including three output buffers, there is no information about only the prescaler consumption.

**simulated results, the chip was fabricated and for the data of writing of this paper is not tested yet.

5. REFERENCES


