Some Techniques to Improve the Performance of Delta-Sigma Modulators

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SUMMARY

In this paper some new and/or modified topologies for multi-bit ΔΣ A/D modulators will be shown. The main results are proven by means of extensive high-level simulations, modeling non-idealities in devices.

First, novel results are presented showing that requantization is feasible. The proposed system is stable for a 1-bit DAC only if the truncation error (T) is shaped with a first order loop. Comparing results with other structures, this one is especially well suited to be implemented with low-resolution analog components. For low oversampling ratios (OSR) the structure presents better performance than the Leslie-Singh’s [1] structure, because the difference between the analog and the digital transfer functions that the truncation error follows to the output is also shaped by a first order digital ΔΣ modulator.

Next, a structure that allows low distortion is presented. The architecture could be considered as an extension of the Chain Of Integrators with Distributed Feedback [3] topology, mixed with the low distortion topology of the Silva’s structure [4].

The use of spatial redundancy is also studied, which can improve the robustness under noisy conditions. Some related results are provided.

Also it is shown that the use of a non uniform quantizer which follows a linear step increase can improve the Dynamic Range (DR) with a little penalty in the Signal to Noise Ratio (SNR) of the system.

Finally the idea of Pseudo-Tangential Noise Transfer Function (PT-NTF) modulators is given. Useful for multi-bit modulators, this technique can provide a moderate increase in the overall SNR with only a little modification in the coefficients of the low pass filter (integrators) of the modulator.

RESUMEN

En este trabajo serán tratadas algunas nuevas y/o modificadas topologías para moduladores ΔΣ del tipo multi-bit. Los principales resultados son corroborados por medio de extensas simulaciones de alto nivel, modelando no idealidades en los dispositivos.

Primero serán presentados nuevos resultados mostrando que la recuantización es factible. El sistema propuesto es estable con el uso de 1-bit DAC si el error de truncamiento (T) es pasado a través de un lazo de primer orden. Comparando resultados con otras estructuras, ésta presenta características especiales para ser implementada con componentes analógicos de baja resolución. Para bajas razones de sobremuestreo (OSR) la estructura presenta mejor performance que la estructura de Leslie & Singh [1], porque la diferencia entre las funciones de transferencia analógica y digital que el error de truncamiento sigue hacia la salida, son procesadas por un modulador digital ΔΣ de primer orden.

Seguidamente una estructura que permite baja distorsión es presentada. Esta configuración puede ser considerada como una extensión de la Cadena de Integradores con Realimentación Distribuida [3], en conjunto con la topología de baja distorsión de la estructura presentada por Silva [4].

El uso de redundancia espacial es también tratado. El mismo puede mejorar la confiabilidad del sistema en condiciones de ruido intenso (como ser ambientes radioactivos). Algunos resultados relacionados son provistos.

Es también mostrado que el uso de un cuantizador no uniforme el cual sigue un incremento lineal en el error puede mejorar el rango dinámico de entrada (DR) deteriorando en mucha menor medida la relación de Señal a Ruido (SNR).

Finalmente la idea de un modulador con Función de Transferencia de Ruido (NTF) del tipo Pseudo-Tangencial es propuesta. Pruebaosha para moduladores multi-bit, esta técnica puede incrementar la SNR con solo una pequeña modificación de los coeficientes en el filtro pasabajos (integradores) del modulador.
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1. INTRODUCTION

Considering non idealities in ΔΣ modulators is an interesting point of study, keeping in mind that the actual trend is to push specific technologies to the limit of their capabilities (cost reasons dictate this procedure). In this article novel concepts are discussed that can improve some aspects of the modulators. Of course there are tradeoffs that must be accomplished in order to obtain improved performance.

The paper presents high-level simulations, carried out with Matlab–Simulink®. The models used have reflected finite DC gain, offset, saturation and non-linear transfer characteristics for the OPAMPs. Also, non ideal capacitor ratios were included, considering future Switched-Capacitor implementations of the architectures.

2. NOVEL CONFIGURATIONS

2.1 Multibit ADC, Single-bit DAC Delta-Sigma Modulator

The use of 1-bit DAC in multi-bit ΔΣ modulators has been a theme of relative high importance, since it ideally allows the good resolution provided by the multibit output and at the same time has the DAC linearity issue solved. In previous relevant works some architectures were presented which performed 1-bit DAC feedback and compensated in the digital domain for truncation [1], or others that used 2 feedback loops (or dual path) [2], being the inner multibit and the outer single bit. In this paper we propose a combination of these architectures in order to obtain insensitivity to analog imperfections.

The blocks diagram for the structure is depicted in the Fig. 1-a, where the basic idea of the proposed requantization loop and the whole functionality can be explained as follows: The most significant bit (MSB) is feedback, previously requantizing the error of this truncation operation. Digital information can be taken and be digitally processed in order to cancel out this truncation shaped error. In previous structures [1], this kind of cancellation was based on the exact matching of the analog and digital transfer functions that this error followed to the final output, but in the present work a difference of matching is always shaped by a first order shaping function (sin(x)), being then the structure more insensitive to analog imperfections. In order to explain these facts consider Fig. 1-b, which presents the simplified linear model of the proposed architecture. Using first order shaping functions (for the sake of simplicity), then:

\[ H_A \equiv H_D \equiv H \equiv \frac{1}{z-1} \]  (1)

Then, the following relations remain:
Fig. 1: a) Proposed architecture. It is composed of an analog delta-sigma loop, with a digital delta-sigma in the feedback path. The truncation error is digitally compensated at the output-summing node. b) Simplified linear model of the whole modulator.

Fig. 2: Structures to replace the B-bits ADC, shaping the quantization noise while preserving a Noise Transfer Function (NTF) equal to 1. a) Silva’s structure b) Error Feedback configuration [3].

\[
H \frac{1}{1+H} z = \frac{z-1}{z}
\]

It must be noted that the truncation error (T) appears at the output of the 1-bit DAC (the summing node of the main feedback loop) multiplied by a second order function, and following the 1-bit ADC Lee’s criterion this point of the circuit is the “problematic” one.

The dithering noise (d) [3] is used to uniform the use of the quantizer levels. It is previously shaped in order to move its power spectral density toward out-of-band frequencies.

\[
Out = \text{in} + \frac{q}{1+H_A} + \frac{d}{(1+H_D)(1+H_A)} + \frac{T}{(1+H_D)} \left( \frac{H_D}{1+H_D} - \frac{H_A}{1+H_A} \right)
\]

Equation (4) is for the ideal first order case meanwhile that equation (3) represents the general one. From this last one it can be easily inferred the previous assumptions about shaping for the truncation noise (T).

Of course the use of multibit quantizers improves the performance of the modulator. Considering now this block, it can be replaced by a more elaborated block that performs the quantization, but in such a way that it has the following STF (Signal Transfer Function) and NTF (Noise Transfer Function):

\[
\text{STF} = 1
\]

\[
\text{NTF} = \left( \frac{z-1}{z} \right)^n \text{ with } n \geq 0
\]

Under these assumptions now the quantization noise can be shaped by a higher order loop. Hence the new delta-sigma can be viewed as a feedback loop that can be added over any stable n-th order conventional delta-sigma. Moreover, because the added sigma-delta is in the forward path, the nonlinearities introduced by a B-bit DAC (which is part of
this last component) are reduced by the outer-loop gain. Then the requirements for the ADC and the DAC used in the inner-loop delta-sigma can be reduced considerably, and also, instead of using a conventional modulator, if the gain of the integrator $H_A$ is enough, analog error-feedback can be tolerated. Some of the proposed possibilities are depicted in Fig. 2-a and 2-b.

In the following analysis and simulation results it will be supposed a bipolar normalized-to-one input and a 5-bits quantizer that saturates at values of ±2.

For the simulations they were used nonlinear models for the analog integrators, which include saturation, nonlinear Opamp DC transfer characteristic and offset. Fig. 3 plots a typical 32768 points FFT response of the simulated structures ([1] and proposed) with Opamp gain=60 dB and with 1mV offset. Clearly, for low OSR there is a big improvement.

If instead of using a single-bit DAC it is used a multi-bit one, still the number of levels can be reduced using a requantization scheme. The behavior of the system is totally nonlinear. As an example for a 5-bit quantizer, if it is used a second order filter for the quantization error, the minimum number of level in the DAC required for stable operation is 10 (roughly 3½ bits). Meanwhile for the same situation in the quantizer, but having second order shaping functions in both the quantizer and the truncation error, the number of needed levels in the DAC grows to 20.

### 2.2 Nested Delta-Sigma Modulators

This paragraph presents a cascade realization in order to obtain a high-order multi-bit delta-sigma modulator. The main advantage of such configuration is that it is composed of similar structures; hence it presents a modular topology, which allows easy implementation and testability at the same time. All the sections are first (or second) order.

Considering the block diagram of Fig. 4 [4], it can be easily proven that it is equivalent of having a signal that pass trough an unitary Signal Transfer Function (STF) added with a noise that comes from a Noise Transfer Function (NTF) equal to $1/(1+H)$, where $H$ is defined to be equal to:

$$ H = \frac{z^{-1}}{z^{-1} - 1} \quad \text{or} \quad H = \frac{2z^{-1} - z^{-2}}{(z^{-1} - 1)^2} \quad (6) $$

For first or second order noise shaping respectively.

Considering now the schematic of the Fig. 5-a, where there was cascaded this structure N times, this is equivalent to consider that the quantization error has been shaped N times too. If it is redraw for the sake of simplicity as in Fig. 5-b, then applying Mason’s rule it can be seen that the output due to the input and due to the quantization error respond to:

$$ V = U \sum_{i=0}^{N} \binom{N}{i} H^i + Q \frac{1}{1 + \sum_{i=1}^{N} \binom{N}{i} H^i} \quad (7) $$

Where the evaluation of the combinatorial give simply perfect polynomials. Then, for the first order $H$ case:

$$ V = STF \cdot U + NTF^N \cdot Q = U + (1 - z^{-1})^W \quad (8) $$
Simulations have shown the feasibility of the proposed architecture. Fig. 6 shows the output spectrum of a first order H cascaded 4 times (ADC=5-bits, Opamp gain=50dB, offset=1mV, DAC nonlinearity=10-bits).

2.3 Spatial Redundancy in Modulators.
The use of spatial redundancy, as depicted in Fig. 7, has the advantage of robustness. At the same time, complexity in the digital domain and more area are obtained as drawbacks. Fig. 8 shows the FFT of the simulated response for a second order modulator using 16 “1 ½ bits” (inset of the figure) comparators, compared against the same scheme but using a 3-bit quantizer. In order to be functional, the architecture needs also K dithering sources, to decorrelate the quantizer outputs. Under this condition, then the output is given by:

\[ V = STF U + NTF \left( \frac{\sqrt{Q}}{\sqrt{K}} \right) = U + \left( 1 - z^{-1} \right) \left( \frac{\sqrt{Q}}{\sqrt{K}} \right) \]  

(9)

Clearly seen in the figure is the fact that there is no visible difference between both configurations.

2.4 Non-Uniform Quantizers
The use of non-uniform quantizer has been addressed in many publications. What is proposed now is to non-uniform in such a way that the step increase follows a linear relationship, as depicted in fig. 9-a. Under these assumptions, nonlinear issues can be greatly reduced. The price to be paid is more complexity in the digital domain, besides of an adaptive dithering scheme. Fig. 9-b shows the simulation results of the proposed quantizer (Fig. 9-a), together with the response of a conventional 3-bit DAC. Clearly there is an improvement of about 75% (5 dB) in the Input Dynamic Range, and a loss of about 2dB only for input values grater than -7dB (normalized to 1, equivalent to 0.4 in linear scale).

2.5 Pseudo-Tangential NTF Modulators
Commonly known fact is that the shape of Noise Transfer Functions (NTF) without zeros-optimization procedures follows sinusoidal shapes (with different order).
The presented idea is to try a different trigonometric function to move the low frequency components of the noise to the upper part of the spectrum. At a first glance, a tangential NTF could accomplish this task with really high performance as can be inferred from the Fig. 10.

Of course, as it can also be seen, for frequencies near half the sampling frequency (fs/2) the gain for the noise tends to infinity, meaning instability. This fact can also be proven using a linear model based in Fig. 4 (because it is used a multi-bit quantizer the linearization is a good approximation for stability purposes). The stability region for a second order system, according with the low-pass filtering function (12), is depicted in Fig. 11:

\[ H(z) = \frac{az + b}{(z-1)^2} \]  

(12)

There are also shown the points for a second order sinusoidal shaping and the tangential one (which lies in the corner of stability). Then the next step is to propose a pseudo-tangential filtering, reducing a little the noise at high frequencies. The price to be paid for such an aggressive NTF is the reduction of the input dynamic range.

Fig. 12 shows the simulation results using the following conditions:

- a=2 b=-1 (conventional)
- a=3 b=-0.75 (proposed)
- OSR=64, Input=0.7 (norm), Resolution=5 bits.

It is easily seen the improvement obtained. As a tradeoff, the stability margins are reduced, but inside certain limits this is not of big concern when dealing with multibit quantizers.

3. CONCLUSIONS

Novel topologies have been presented and simulations results provided to improve the performance of this kind of modulators. The next step is the fabrication of prototypes to validate experimentally all the concepts.

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